REMARKS

Claims 1-11 remain in this application. Claims 4-5 and 6-7 have been amended. Independent claims 4 and 6 have been amended by replacing "a terminal resistor" with "a plurality of terminal resistors", and "the terminal resistor" with "the plurality of terminal resistors". Claims 5 and 7 have been amended by replacing "the terminal resistor" with "the plurality of terminal resistors". Claims 10-11 have been added; these claims are patentable for the reasons set out below. Claim 10 is supported in the specification at page 7, lines 5-6. Claim 11 is supported at page 7, lines 24-30, and in Fig. 4. In response to the Official Action:

35 U.S.C. 112

Claims 5 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

The Applicant has amended the claims to recite "a plurality of terminal resistors" to overcome this rejection, withdrawal of which is solicited.

35 U.S.C. 102(b)

Claim 1 was rejected under 35 U.S.C. 102(b) as being anticipated by Cronin (U.S. Patent 6,128,685). This rejection is respectfully traversed.

Claim 1. Claim 1 recites a motherboard, comprising a printed circuit board; a first memory slot set disposed on the printed circuit board having a first memory slot and a second memory slot; a second memory slot set disposed on the printed circuit board having a third memory slot and a fourth memory slot; and a terminator circuit module disposed between the first memory slot set and the second memory slot set, wherein the terminator circuit module is

electrically connected to the first memory slot set and the second memory slot set through the printed circuit board.

Cronin does not teach or suggest a first memory slot set and a second memory slot set.

Claim 1 recites a first memory slot set disposed on the printed circuit board having a first memory slot and a second memory slot and a second memory slot set disposed on the printed circuit board having a third memory slot and a fourth memory slot. It would have been obvious to one skilled in the art that *the four memory slots recited in claim 1 are designed for memory devices.*

Cronin discloses a printed circuit board 120 comprising a motherboard, having a processor bus 25 (column 6, lines 67), and the processor bus 25 is coupled to four connectors 130a-130d (column 7, lines 3-4). But in column 7, lines 10-13, Cronin recites that each connector 130 may comprise a slot having connector contacts 131 configured to engage corresponding contact 63 of a processor card 62 which supports the processor 160. Cronin clearly states that *the four connectors 130a-130d are designed for the processors, not for the memory devices.*

Indeed, in Cronin's applied Fig. 4 the memory 22 (column 7, line 9) is on the motherboard 120 while the inserted processor card 62 has a processor 160 (column 7, line 11), and card 140 has termination circuits 70 which "terminate the processor bus 25" (column 7, lines 20-23). (Cronin also states at column 7, line 15, that card 62 includes termination circuits that are "not shown".) The device 71 is not explained in relation to applied Fig. 4, but is called an "auxiliary circuit" in relation to Fig. 10 (column 8, line 64).

The devices 23 shown between the connectors are "chipsets." The bus 25 is "terminated on one side of the chipset 23. The bus is terminated on the opposite side of the chipset 23 by the support member 140 which has termination circuits 70 thereon" (column 7, lines 17). Clearly, the chipset 23, being between the bus and the termination, is not itself a terminator.

With respect, the four connectors 130a-130d are not a "memory slot set" as the Examiner asserts, because the memory is not on the cards inserted into them; the memory is on the board. Furthermore, the asserted terminator circuit module 23 is actually a chipset which is between the termination circuit and the bus.

For this reason alone, the Applicant believes that claim 1 is allowable over the cited reference. Thus, the Applicant believes that claim 1 is allowable over the cited references. Insofar as claim 1 is allowable, claims 2-3 and 10-11, all depending from claim 1 and its related claims, are allowable, and are also allowable on their own merits in claiming additional elements not included in claim 1.

35 U.S.C. 103(a)

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cronin (U.S. Patent 6,128,685) in view of Bennett et al. (U.S. Patent 5,747,893). This rejection is respectfully traversed.

Claim 2. Claim 2 recites the motherboard as claimed in claim 1, wherein the terminator circuit module comprises a plurality of resistors and a plurality of capacitors, and the plurality of resistors and the plurality of capacitors are connected in series.

Neither Cronin nor Bennett teaches, discloses or suggests a plurality of resistors and a plurality of capacitors connected in series.

As the Examiner states, Cronin does not disclose a plurality of resistors and a plurality of capacitors connected in series. It discloses one resistor and capacitor in parallel (Fig. 3). The Examiner relies on Bennett.

In Fig.2 of Bennett, the resistor R_{ZN1} and capacitor C_1 are connected in series, and the resistor R_{ZN2} and capacitor C_2 are also connected in series. However, *one end of each capacitor*

C_1 and C_2 is connected to ground. Therefore, Bennett's resistor-capacitor sets are *not* connected in series, they are connected in parallel. This is contrary to the language of claim 2.

For this reason alone, the Applicant believes that claim 2 is allowable over the cited reference. Thus, the Applicant believes that claim 2 is allowable over the cited references. Insofar as claim 2 is allowable, claims 3 and 11, all depending from claim 2 and its related claims, are allowable, and are also allowable on their own merits in claiming additional elements not included in claim 2.

35 U.S.C. 103(a)

Claims 4, 6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (figure 1-2) in view of Fan (U.S. Patent 6,665,736). This rejection is respectfully traversed.

Claim 4. Claim 4 recites a motherboard, comprising a circuit board; a chipset disposed on the circuit board; a first memory slot set disposed on the circuit board having a first memory slot and a second memory slot; a second memory slot set disposed on the circuit board having a third memory slot and a fourth memory slot; a plurality of terminal resistors disposed between the first memory slot set and the second memory slot set; and a serial resistance disposed between the chipset and the first and the second memory slot sets, wherein the plurality of terminal resistors is electrically connected to the first memory slot set and the second memory slot set through the circuit board, and the plurality of terminal resistors, the first memory slot set and the second memory slot set are connected to a terminator voltage.

Neither AAPA nor Fan teach, disclose or suggest *a plurality of terminal resistors, a first memory slot set and a second memory slot set are connected to a terminator voltage.*

Although there is a resistor RS positioned between the SDR DIMM slot 504 and DDR DIMM slot 505, *there is no terminator voltage coupled to the resistor RS, SDR DIMM slot 504 and DDR DIMM slot 505* (see Fig. 5A of Fan).

For this reason alone, the Applicant believes that claim 4 is allowable over the cited reference. Thus, the Applicant believes that claim 4 is allowable over the cited references. Insofar as claim 4 is allowable, claims 5 depend from claim 4 and its related claims, are allowable, and are also allowable on their own merits in claiming additional elements not included in claim 4.

Claim 6. Claim 6 recites a slot apparatus for a memory module on a printed circuit board, comprising a first memory slot set disposed on the printed circuit board having a first memory slot and a second memory slot; a second memory slot set disposed on the printed circuit board having a third memory slot and a fourth memory slot; a plurality of terminal resistors disposed between the first memory slot set and the second memory slot set; and a serial resistance disposed on the printed circuit board and electrically connected to the first memory slot set and the second memory slot set through the printed circuit board, wherein the plurality of terminal resistors is respectively and electrically connected to the first memory slot set and the second memory slot set through the printed circuit board, and the terminal resistor, the first memory slot set and the second memory slot set are connected to a terminator voltage.

Neither AAPA nor Fan teaches, discloses or suggests *a plurality of terminal resistors, a first memory slot set and a second memory slot set connected to a terminator voltage.*

Although Fan discloses a resistor RS positioned between the SDR DIMM slot 504 and DDR DIMM slot 505, *there exists no terminator voltage coupled to the resistor RS, SDR DIMM slot 504 and DDR DIMM slot 505* (see Fig. 5A of Fan).

For this reason alone, The Applicant believes that claim 6 is allowable over the cited reference. Thus, the Applicant believes that claim 6 is allowable over the cited references.

Insofar as claim 6 is allowable, claims 7-9, all depend from claim 6 and its related claims, are allowable, and are also allowable in claiming elements not included in claim 6.

35 U.S.C. 103(a)

Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (figure 1-2), Fan (U.S. Patent 6,665,736) and Bennett et. al. (U.S. Patent 5,747,893).

Claim 5. Claim 5 recites the motherboard as claimed in claim 4, further comprising a plurality of capacitors, wherein the plurality of terminal resistors and the plurality of capacitors are alternately arranged.

Neither AAPA, Fan nor Bennett teaches, discloses or suggests a capacitor connected to a resistor formed in the terminal resistor in series.

As noted above, Fig.2 of Bennett shows that the resistor R_{ZN1} and capacitor C_1 are connected in series, and the resistor R_{ZN2} and capacitor C_2 are also connected in series. However, *one end of each capacitor C_1 and C_2 is connected to ground.* Therefore, Bennett's resistor-capacitor sets are *not* connected in series, they are connected in parallel. Moreover, as shown in Fig.2 of Bennett, there is no terminator voltage connected to the resistors R_{ZN1} and R_{ZN2}.

For this reason alone, the Applicant believes that claim 5 is allowable over the cited reference.

Claim 7. Claim 7 recites the slot apparatus for a memory module as claimed in claim 6, further comprising a plurality of capacitors, wherein the plurality of terminal resistors and the plurality of capacitors are alternately arranged.

Neither AAPA, Fan, nor Bennett teaches, discloses, or suggests a capacitor connected to a resistor formed in the terminal resistor in series.

As noted above, Fig.2 of Bennett shows that the resistor R_{ZN1} and capacitor C_1 are connected in series, and the resistor R_{ZN2} and capacitor C_2 are also connected in series. However,

one end of each capacitor C_1 and C_2 is connected to ground. Therefore, Bennett's resistor-capacitor sets are *not* connected in series, they are connected in parallel. Moreover, as shown in Fig.2 of Bennett, there is no terminator voltage connected to the resistors R_{ZN1} and R_{ZN2}.

For this reason alone, the Applicant believes that claim 7 is allowable over the cited reference.

New Claims. The new claims 10-11 recite, in part, "wherein the first, second, third and fourth memory slot are used for plugging in a memory device" and "wherein the terminator circuit module further comprises a terminator voltage connected to the first memory slot set, the second memory slot set and the plurality of resistors." In view of the discussion above, the Applicant believes that it is clear that these limitations are not taught by the applied references.

Conclusion. For the reasons as described above, the Applicant believes that claims 1, 4 and 6 are allowable over the references. Insofar as claim 1 is allowable, claims 2-3, and 10-11, all depend from claim 1 and its related claims, including every claimed element thereof, are also allowable on their own merits in claiming additional elements not included in claim 1. For the reasons described above, the Applicant believes that claim 4 is allowable. Insofar as claim 5 depends from claim 4 and its related claims, they are also allowable. Moreover, for the reasons as described above, the Applicant believes that claim 6 is allowable. Insofar as claims 7-9 depend from claim 6 and its related claims, they are also allowable.

Withdrawal of the rejections is respectfully requested. The Applicant has made every effort to place the present application in condition for allowance. It is therefore earnestly requested that the present application, as a whole, receive favorable consideration and that all of the claims be allowed in their present form.

Should Examiner feel that further discussion of the application and the Amendment is conducive to prosecution and allowance thereof, please do not hesitate to contact the undersigned at the address and telephone listed below.

Respectfully submitted,

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Date

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